WHAT IS CLAIMED IS:

1. An array substrate for use in an in-plane switching liquid crystal display device, comprising:

a plurality of gate lines having a first direction on a substrate;

a plurality of data lines having a second direction substantially perpendicular to the plurality of gate lines, wherein pairs of the gate and data lines define a pixel region;

a common line disposed in the first direction between the plurality of gate lines;

a plurality of common electrodes extending from the common line in the pixel region, wherein the common electrodes have an arc shape;

thin film transistors disposed at four corners of the pixel region near crossings of the gate and data lines;

a capacitor electrode above a portion of the common electrodes, wherein the capacitor electrode is connected to a corresponding thin film transistor; and

a plurality of pixel electrodes connected to the capacitor electrode and disposed between the arc shape of the common electrodes, wherein the pixel electrodes are arc shaped,

wherein the pixel region is divided into a plurality of sub pixels, each of which includes one thin film transistor, at least one capacitor electrode, and at least one pixel electrode.

2. The array substrate of claim 1, wherein each of the plurality of data lines is adjacent to a data line of a neighboring pixel and each of the gate lines is adjacent to a gate line of a neighboring pixel.

3. The array substrate of claim 1, wherein the pixel region is divided into red, green, blue and white sub pixels.

4. The array substrate of claim 1, wherein the pixel region is divided into red, green and blue sub pixels.

5. The array substrate of claim 1, wherein the common electrodes are divided into two parts each having a semicircular shape.

6. The array substrate of claim 5, wherein the common electrodes include a first common electrode pattern surrounding peripheries of the pixel region, the first common electrode pattern having a circular opening in a middle portion thereof.

7. The array substrate of claim 6, wherein the common electrodes further include second and third common electrode patterns inside the circular opening.

8. The array substrate of claim 7, further comprising a pixel connecting line, wherein the pixel connecting line extends from the capacitor electrode, and wherein the pixel electrode is connected to the pixel connecting line.

9. The array substrate of claim 8, wherein the pixel electrode includes a first pixel electrode pattern between the first and second common electrode patterns and a second pixel electrode pattern between the second and third common electrode patterns.

10. The array substrate of claim 9, wherein the pixel electrode is in each of the plurality of sub pixels.

11. The array substrate of claim 10, wherein the capacitor electrode and the first common electrode pattern form a storage capacitor.

12. The array substrate of claim 11, further comprising a black matrix covering a portion corresponding to the gate and data lines, the thin film transistor, and the pixel connecting line.

13. The array substrate of claim 1, wherein the plurality of sub pixels are substantially circular shaped.

14. The array substrate of claim 13, wherein there are at least four sub pixels.

15. The array substrate of claim 1, wherein each of the plurality of the sub pixels is symmetric to an adjacent sub pixel.

16. The array substrate of claim 15, wherein thin film transistors in each of the plurality of sub pixels are symmetric with respect to the common line.

17. A method of forming an array substrate for use in an in-plane switching liquid crystal display device, comprising;

forming gate lines, common lines, gate electrodes, and common electrodes, wherein the common line is disposed between two gate lines, the gate electrode extends from the gate lines toward the common line, and the common electrode extending from the common line is arc shaped;

forming a gate insulating layer on the gate lines, common lines, gate electrodes, and common electrodes;

forming a semiconductor layer on the gate insulating layer, the semiconductor layer including a first layer of pure amorphous silicon and a second layer of doped amorphous silicon;

forming data lines, source electrodes and drain electrodes, wherein the data lines are substantially perpendicular to and cross the gate and common lines, each of the source electrodes extending from the data lines over a first end portion of the semiconductor layer, each of the drain electrodes being spaced from a corresponding source electrode and overlapping a second end portion of the semiconductor layer, and pairs of the gate and data lines defining a pixel region, wherein the pixel region is divided into a plurality of sub pixels;

forming a passivation layer on the data lines, the source electrodes and the drain electrodes, the passivation layer having drain contact holes exposing a portion of the drain electrodes; and

forming capacitor electrodes and pixel electrodes, the capacitor electrodes being disposed over a portion of the common electrodes and in contact with the drain electrodes

through the drain contact holes in each of the sub pixels, wherein the pixel electrodes are connected to the capacitor electrodes in each of the sub pixels through a pixel connecting line,

wherein the common electrodes and the pixel electrodes are arc shaped within the pixel region.

18. The method of claim 17, wherein each of the data lines is disposed adjacent to a data line of a neighboring pixel and each of the gate lines is disposed adjacent to a gate line of a neighboring pixel.

19. The method of claim 17, wherein the pixel region is divided into red, green, blue and white sub pixels.

20. The method of claim 17, wherein the pixel region is divided into red, green and blue sub pixels.

21. The method of claim 17, wherein the common electrodes are divided into two parts, each having a semicircular shape.

22. The method of claim 21, wherein the common electrodes include a first common electrode pattern surrounding peripheries of the pixel region, the first common electrode pattern having a circular opening.

23. The method of claim 22, wherein the common electrodes further include second and

third common electrode patterns inside the circular opening.

24. The method of claim 23, wherein the pixel connecting line extends from the capacitor electrodes, and the pixel electrodes extend from the pixel connecting line.

25. The method of claim 24, wherein the pixel electrodes include a first pixel electrode pattern between the first and second common electrode patterns and a second pixel electrode pattern between the second and third common electrode patterns.

26. The method of claim 25, wherein the capacitor electrode and the first common electrode pattern form a storage capacitor.

27. The method of claim 25, wherein each sub pixel has a pixel electrode.

28. The method of claim 25, wherein the pixel electrodes are simultaneously formed in each of the sub pixels.

29. The method of claim 17, further comprising forming a black matrix covering a portion corresponding to the gate and data lines, a thin film transistor, and the pixel connecting line.